IN THE SPECIFICATION

On page 1, fourth paragraph, the paragraph has been amended as follows:

On the other hand, because the DLL is less affected by noise compared to a PLL(Phase Locked Loop), it is ~~wildly~~ widely used for a synchronous semiconductor memory such as a DDR SDRAM(Double Data Rate Synchronous DRAM). Among some kinds of the DLL, a register controlled DLL is a most typically used DLL is.

On page 10, first paragraph, the paragraph has been amended as follows:

Referring to Fig. ~~5~~5A, the decoding unit 42 includes a plurality of 3-input NAND gates ND1, ND2, ND3, ND4, each for receiving the test mode signal tm_en as its one input and one of the combinations of the address signals A0, A1 and the inverted address signals Ab0, Ab1 as the other input, and a number of inverters I3, I4, I5, I6 for inverting the output signals of the NAND gates ND1, ND2, ND3, ND4.